## REMARKS

Claims 1, 17, 18, 22, 24 and 26 are amended. Claims 1-26 remain in the application.

The amendments to claims 17, 22 and 26 are made to eliminate a redundant word. These amendments are voluntary; they are not made to support patentability or evade prior art. Accordingly, these amendments do not reduce the scope of equivalents to which the applicant is entitled.

Claims 1, 18, and 24 have been amended to recite "embedding operating speed instructions" in a program or a Java applet "to be used by a microprocessor executing the program to achieve a level of performance required by the program." These amendments are supported in the specification at paragraphs [0020] and [0021] and do not introduce new matter into the application.

Claims 1-17 and 24-16 are rejected for obviousness over the applicants' admitted prior art in view of US Patent 5790877 ("Nishiyama"). That rejection is respectfully traversed for the following reasons.

*Prima facie*, rejection of a claim for obviousness over a combination of references requires some motivation to combine the references, a reasonable expectation of success, and the inclusion of all elements of the rejected claim in the combination. See MPEP 2143, et seq.

Taking claim 1 as representative, a method to control the operating speed of a microprocessor to provide processing power sufficient to run a program while a predetermined level of performance is maintained includes "embedding operating speed instructions in a program to be used by a microprocessor executing the program to achieve a level of performance required by the program", reading the embedded instructions and adjusting the operating speed accordingly. Claim 24 recites a system for controlling the operating speed of a microprocessor that includes a "means for downloading a program embedded with operating speed instructions to be executed by a microprocessor to achieve a level of performance required by the program".

Nishiyama sets forth a method for controlling a processor to save power during program execution. During compilation of a program, a compiler detects hardware resources needed to execute instructions of the program. Based upon hardware needs it has detected, the compiler generates clock control instructions to modulate clock speed of the processor during program execution and places them in the compiled program. See Nishiyama at col. 2, lines 44-51. The program acted upon by the compiler has no

clock frequency instructions (Nishiyama at col. 4, line 60 through col. 6, line 1). The compiled program produced by the compiler has clock frequency instructions, but they have been put there by the compiler in response to the contents of a resource utilization table 504 which is probably a component of the compiler. The resource conservation controls implemented by the clock control instructions are inherent in the compiler and the resource utilization table; they are external to the un-compiled program and its compiled counterpart. The compiler and the resource utilization table implement hardware requirements, external to any program, and transcendent over all programs acted on by the compiler and the table and executed by the hardware. They do not embed any instructions to "achieve a level of performance required by the program." The proposed combination therefore does not teach or suggest embedding operating speed instructions in a program in order to operate a microprocessor to "achieve a level of performance required by the program."

Further, claim 10 further limits the method of claim 1 by reciting that the "instructions are embedded by the creator of the program". Neither the compiler nor the resource utilization table is a "creator" of a program. The compiler merely translates or adapts an existing program; it does not "create" any program.

Finally, respecting claims 17 and 26, it is contended in the Office Action that "it is obvious in the AAPA-Nishiyama system a number of instructions per second to be processed could be specified since it would require adjusting the speed of the processor." The applicant respectfully disagrees. It is one thing to tell a processor at what clock frequency to operate; it is quite another to tell it how many instructions per second to execute. In the first place, the clock speed is fixed by command. In the second case, the clock speed can vary. The applicant therefore requests citation of a reference, entry of an affidavit, or taking Official Notice to support this aspect of the rejection.

Accordingly, for failure of the cited art to include or suggest "embedding operating speed instructions in a program to be used by a microprocessor executing the program to achieve a level of performance required by the program", the combination fails to meet the *prima facie* requirements for obviousness and this rejection should be withdrawn.

Claims 18-23 are rejected for obviousness over the applicant's admitted prior art, Nishiyama, and US Patent 6477654 ("Dean"). That rejection is respectfully traversed for reasons given above in support of the patentability of amended claims 1 and 24, and their dependents. Claim 18 concerns a method to control of the speed of a

microprocessor in executing an applet by "embedding operating speed instructions in a Java applet to be used by a microprocessor to achieve a predetermined level of performance required by the applet", executing the applet, reading the embedded instructions and then "adjusting the speed of the microprocessor in accordance with the instructions from a low-speed, low-power setting to a high-speed, high-power setting such that sufficient processing power is provided to achieve the predetermined level of performance in executing the applet." Like Nishiyama, the power control instructions in Dean's system are inserted during recompilation of a program by an analysis function that analyzes hardware. Thus, the instructions are inserted according to hardware metrics external to the program, not "to achieve a predetermined level of performance required by the applet".

Accordingly, for failure of the cited art to include or suggest "embedding operating speed instructions in a Java applet to be used by a microprocessor executing the program to achieve a level of performance required by the applet", the combination fails to meet the *prima facie* requirements for obviousness and this rejection should be withdrawn.

In view of amendments to claims 1, 18, and 24, and with regard to the remarks in support of patentability it is submitted that the claims of this application are in condition for allowance, early notice of which is earnestly requested.

Respectfully submitted,

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